REMARKS

Claims 1-18 are pending. Claims 8-18 were withdrawn from consideration in response to a restriction requirement. Claims 1-7 were rejected.

Rejection Under 35 U.S.C. §112

The Examiner rejected Claims 4 and 7 under 35 U.S.C. §112 as being indefinite.

The Examiner stated that certain elements of Claim 4 were not materials within the scope of the Markush group in the claim. Claim 4 has been amended to recite material arrangements, thus encompassing all recited elements within the scope of the Markush group. Claims 1-3 and 7 have been amended accordingly. Therefore, it is respectfully requested that the rejection under 35 U.S.C. §112, second paragraph of Claim 4 be withdrawn.

The Examiner stated that Claim 7 failed to define "cross-section surface area of the at least two different materials". Claim 7 has been amended to clarify the definition of the cross-section surface area. Therefore, it is respectfully requested that the rejection under 35 U.S.C. §112, second paragraph of Claim 7 be withdrawn.

Rejections Under 35 U.S.C. §102(b) and 35 U.S.C. §103(a)

The Examiner rejected Claims 1-3 and 6 as being anticipated by U.S. Patent No. 4,851,078 (Short). The Examiner rejected Claim 5 as being unpatentable over Short in view of U.S. Patent No. 5,506,433 (Ohori).

Short discloses a method of forming a high quality dielectrically isolated silicon on insulator semiconductor device using a double wafer bonding process.

Claim 1 has been amended to better claim the invention. The Examiner cites Short as disclosing all elements of independent Claim 1. In particular, the Examiner cites Short at column 4, lines 8-25 and Figures 5-7 as disclosing at least two different materials within a pocket. Most relevantly, Short at column 4, lines 10-21 reads:

> Specifically in FIG. 1, a substrate 10 is provided formed of a low resistivity monocrystalline silicon wafer of N-type conductivity. A layer 15 of heavily doped N-type silicon is provided on the top surface of the substrate 10, which will serve as a

> buried layer in the final product. The N-type layer 15 is then oxidized 20 and patterned for the isolation pattern. Moats or grooves 25 are formed on the surface, as shown in FIG. 4. The moats 25 are then oxidized to provide the oxide layer 28. A thick polycrystalline silicon layer 30 is grown on the surface of oxide layer 28.

The Examiner suggests that the oxide and the polycrystalline silicon constitute two different materials provided within a pocket. However, Short states in the text cited above that the moats 25 are oxidized to provide the oxide layer 28. The oxide is the result of a treatment of pre-existing material, i.e. the monocrystalline silicon wafer that composes the walls of the moats 25, and is not a deposited material arrangement as recited in Claim 1 as amended. Thus, Short does not disclose, either in the above-cited text or anywhere else in the specification, at least two different material arrangements deposited within a pocket as recited by Claim 1 as amended. Therefore, Claim 1 is believed to be allowable over Short.

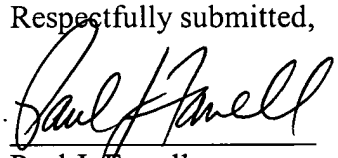
Without conceding patentability per se of dependent Claims 2, 3, and 6, it is respectfully submitted that the rejection under 35 U.S.C. §103(a) of Claims 2, 3, and 6 should be withdrawn by virtue of their dependence on Claim 1.

Without conceding patentability per se of dependent Claim 5, it is respectfully submitted that the rejection under 35 U.S.C. §103(a) of Claim 5 should be withdrawn by virtue of its dependence on Claim 1.

Claim 7 was not rejected over the prior art and is believed to be in allowable condition since the rejection under 35 U.S.C. §112, second paragraph has been addressed.

Applicants submit that pending Claims 1-7 are believed to be in condition for allowance. Allowance is respectfully requested. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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